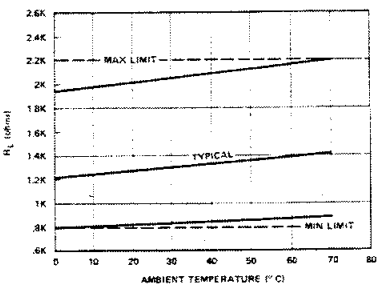
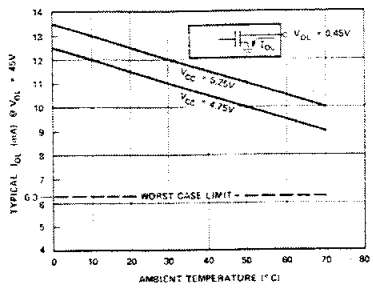
D. C. Characteristics

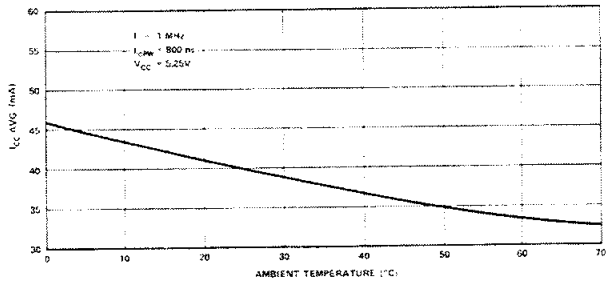
TEMPERATURE DEPENDENCE OF INTERNAL LOAD RESISTORS



TEMPERATURE DEPENDENCE OF OUTPUT LOW LEVEL SINK CAPABILITY

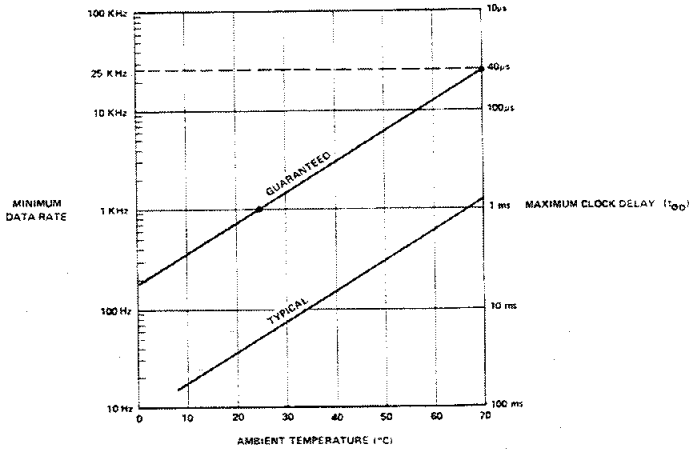


POWER SUPPLY CURRENT (I_{CC}) VS. AMBIENT TEMPERATURE (°C)

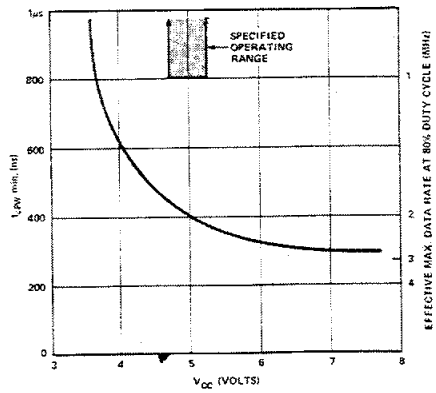


A. C. Characteristics

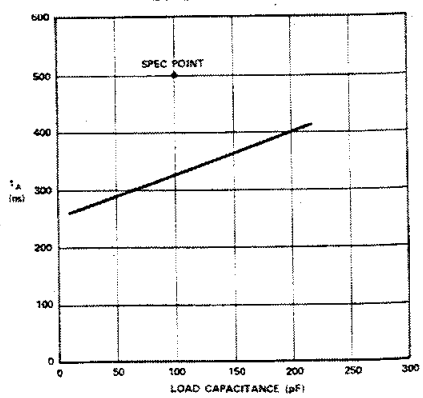
MINIMUM DATA RATE AND MAXIMUM CLOCK DELAY VS. AMBIENT TEMPERATURE



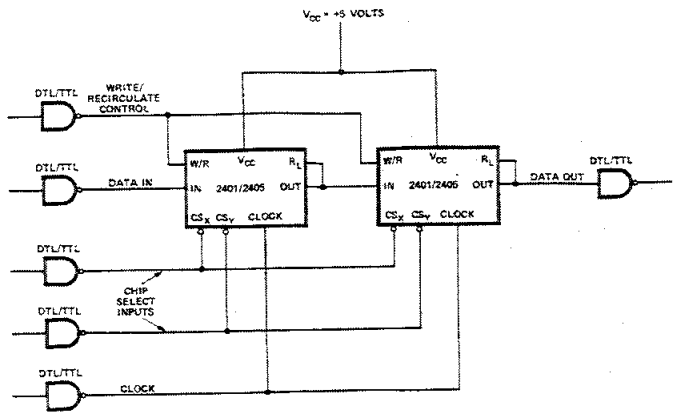
MINIMUM CLOCK PULSE WIDTH AND EFFECTIVE MAXIMUM DATA RATE AT 80% DUTY CYCLE VS. POWER SUPPLY VOLTAGE (V_{CC})



ACCESS TIME VS. LOAD CAPACITANCE



DIRECT TTL COMPATIBLE SHIFT REGISTERS



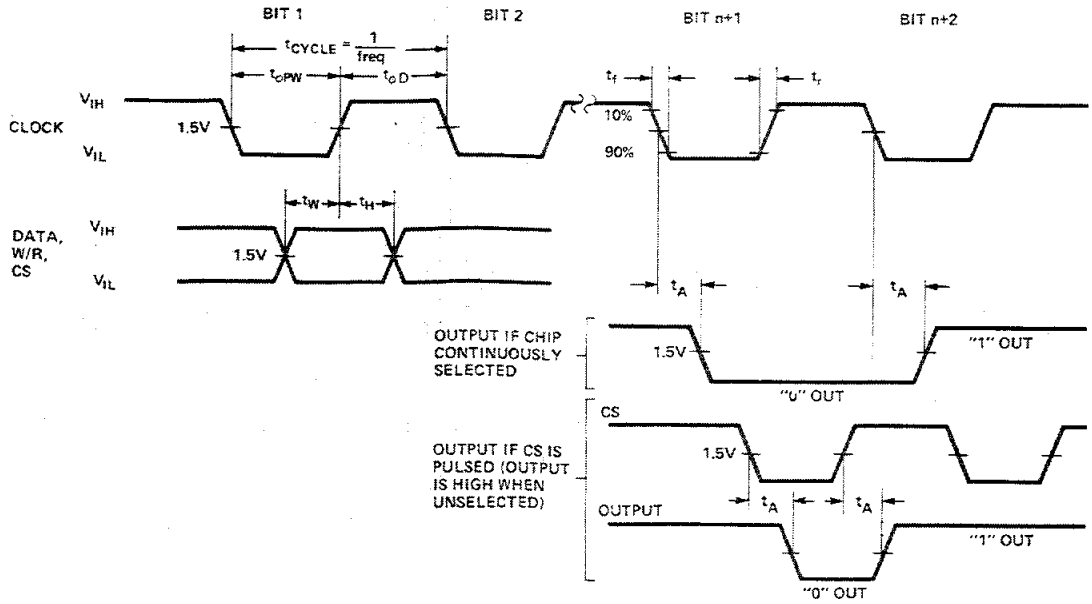
A. C. Characteristics T_A = 0°C to 70°C, V_{CC} = +5V ±5%, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
FREQ. MAX.	MAX. DATA REP. RATE			1	MHz	
FREQ. MIN.	MIN. DATA REP. RATE	1 25			KHz KHz	T_A = 25° C T_A = 70° C
$t_{\phi PW}$	CLOCK PULSE WIDTH	0.80		10	μs	
$t_{\phi D}$	CLOCK PULSE DELAY	0.20 0.20		1000 40	μs μs	T_A = 25° C T_A = 70° C
t_r , t_f	CLOCK RISE AND FALL TIME			50	ns	
t_W	WRITE TIME	200			ns	
t_H	HOLD TIME	150			ns	
t_A	ACCESS TIME FROM CLOCK OR CHIP SELECT		250	500	ns	R_L CONNECTED, C_L = 100 pF ONE TTL LOAD

Capacitance T_A = 25° C

SYMBOL	PARAMETER	LIMITS MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
C_{IN}	DATA, W/R & CS INPUT CAPACITANCE		4	7	pF	ALL PINS AT AC GROUND; 250 mV PEAK TO PEAK, 1 MHz
C_{OUT}	OUTPUT CAPACITANCE		10	14	pF	
C_ϕ	CLOCK CAPACITANCE		4	7	pF	

Waveforms



Absolute Maximum Ratings*

Ambient Temperature Under Bias:	0° C to 70° C
Storage Temperature:	−65° C to +150° C
Power Dissipation:	1W
Voltage on Any Pin with Respect to Ground:	−0.5V to +7V

*COMMENT:

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

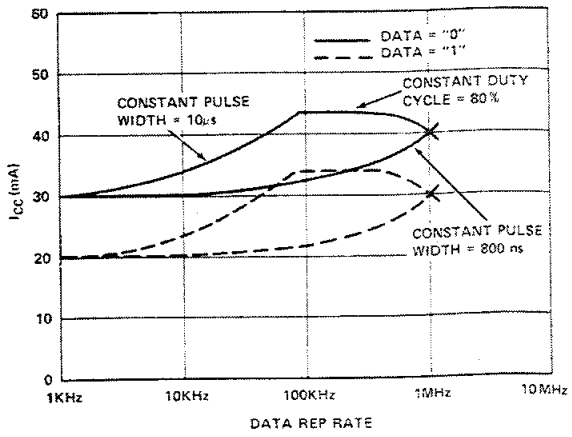
D. C. Characteristics

T_A = 0°to 70°C, V_{CC} = +5V ±5%, unless otherwise specified.

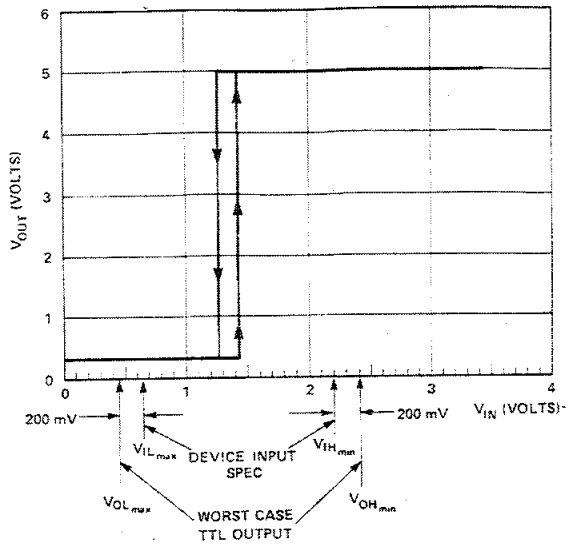
SYMBOL	PARAMETER	LIMITS MIN.	TYP.(1)	MAX.	UNITS	TEST CONDITIONS
I_{LI}	INPUT LEAKAGE			10	μA	V_{IN} = 5.25V
I_{LO}	OUTPUT LEAKAGE			100	μA	V_{OUT} = 5.25V
I_{CC}	POWER SUPPLY CURRENT		45 50	70 80	mA mA	T_A = 25°C, T_A = 0°C; V_{CC} = 5.25V; 80% DUTY CYCLE
V_{IH}	INPUT HIGH LEVEL VOLTAGE (ALL INPUTS)	2.2		5.25	V	
V_{IL}	INPUT LOW LEVEL VOLTAGE (ALL INPUTS)	−0.3		0.65	V	
I_{OL}	OUTPUT LOW SINK CURRENT	6.3	10		mA	V_{OL} = 0.45V
V_{OH}	OUTPUT HIGH LEVEL VOLTAGE	2.4		V_{CC}	V	I_{OH} = -1mA, R_L CONNECTED
V_{OL}	OUTPUT LOW LEVEL VOLTAGE	0		0.45	V	I_{OL} = 1.6 mA, R_L CONNECTED
R_L	INTERNAL LOAD	0.8	1.3	2.2	KΩ	

NOTE (1): Typical values are at 25°C and at nominal voltage.

POWER SUPPLY CURRENT (I_{CC}) VS. DATA REP RATE



EFFECTIVE INPUT CHARACTERISTIC



2048/1024 BIT DYNAMIC RECIRCULATING SHIFT REGISTERS

- **Single Supply Voltage -- +5 Volts**
- **Fully TTL Compatible -- Inputs, Outputs and Clock**
- **Single Phase Clock**
- **Guaranteed 1 MHz Operation with 100 pF Load, over Temperature Range**
- **Low Power Dissipation -- 120 μw/bit typically at 1 MHz**
- **Low Clock Capacitance -- 7 pF**
- **Write/Recirculate and Chip Select Logic Incorporated on Chip**
- **Standard Configurations -- Dual 1024 Bit -- 2401 Single 1024 Bit -- 2405**

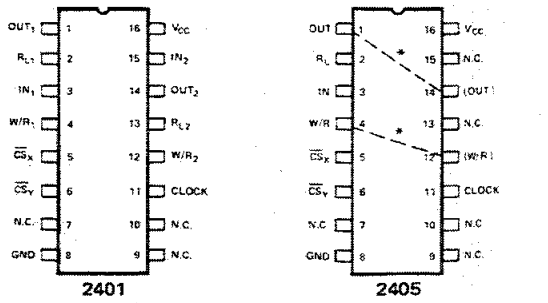
The 2401/2405 are 2048/1024 bit dynamic recirculating shift registers. They are directly TTL compatible in all respects: inputs, outputs, clock and a single +5 volt power supply.

Write/recirculate controls are provided to eliminate the need for external logic elements when recirculating data.

Two chip select inputs have been provided to allow easy selection of an individual package when outputs of several devices have been "OR-tied". A separate internal "pullup" resistor (R_L) is provided which can be externally connected to the output pin to achieve full signal swing.

This Intel shift register family is fabricated with N-channel silicon gate technology. This technology provides the designer with high performance, easy to use MOS circuits. Only a single +5V power supply is needed and all devices are directly TTL compatible, including clocks.

PIN CONFIGURATIONS

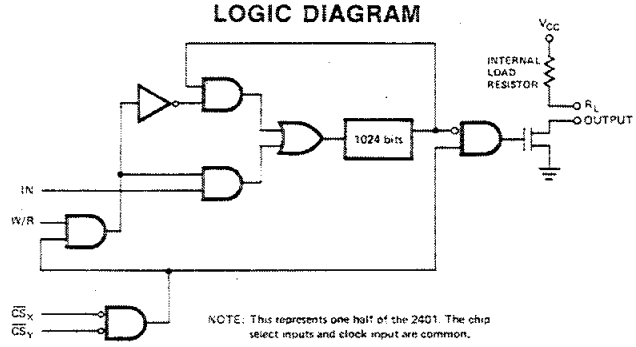


* DASH LINES INDICATE NECESSARY EXTERNAL PRINTED CIRCUIT BOARD CONNECTIONS FOR PROPER OPERATION OF THE 2405. (SEE APPLICATION SECTION)

PIN NAMES

IN	DATA INPUT	OUT	DATA OUTPUT
W/R	WRITE/RECIRCULATE CONTROL	R_L	INTERNAL LOAD RESISTOR
$\overline{CS}_X$, $\overline{CS}_Y$	CHIP SELECT INPUT	N.C.	NO CONNECTION

LOGIC DIAGRAM



NOTE: This represents one half of the 2401. The chip select inputs and clock input are common.

TRUTH TABLE

FUNCTION	PIN SYMBOL W/R	$\overline{CS}_X$	$\overline{CS}_Y$
WRITE MODE	H	L	L
RECIRCULATE	L	X	X
	X	H	X
	X	X	H
READ MODE	X	L	L

H = Logic High Level L = Logic Low Level
X = Don't Care Condition